재료의 전기적 성질

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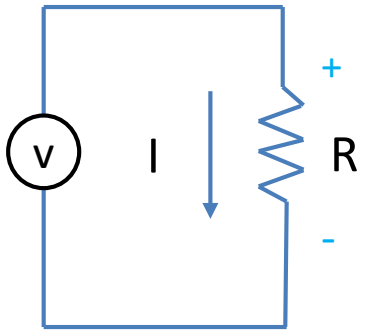
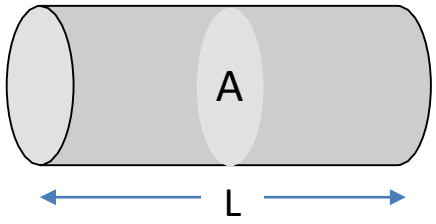
Contents

Ohm's law

Resistivity & Electrical Conductivity





$$R \propto \frac{L}{A}$$

Current [A]

$$V = IR$$

Voltage[V] Resistance [Ω]

Ohm's Law

Resistivity & Electrical Conductivity

- **Resistivity**

$$R = \rho \frac{L}{A}$$ 단위 : $[\Omega \cdot m]$

- **Electrical Conductivity**

$$\sigma = \frac{1}{\rho}$$ 단위 : $[\Omega \cdot m]^{-1}$

J [A/m^2]
Current density

E [V/m]
Electric field intensity

$$\frac{V}{L} = \frac{I}{A}\rho$$

Resistivity [Ω·m]

$$J = \sigma E$$

Current density ∝ Electric field intensity

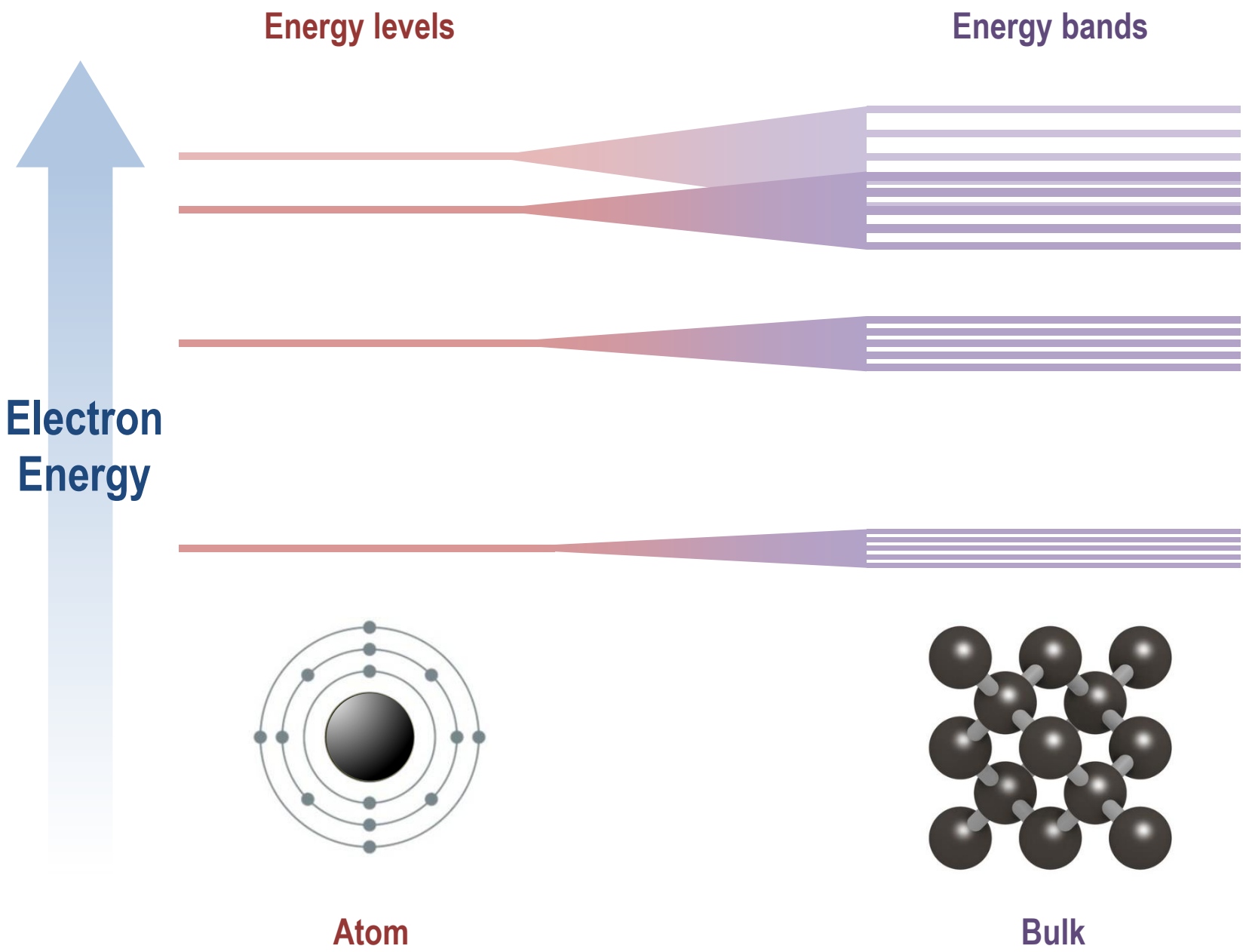
Resistivity & Electrical Conductivity

Conductivity σ

Conductors	Silver	6.8×10^{7}
	Copper	6.0×10^{7}
	Iron	1.0×10^{7}
Semiconductors	Silicon	4.0×10^{-4}
	Germanium	2.0×10^{0}
	GaAs	1.0×10^{-6}
Insulators	Soda-lime glass	1.0×10^{-10}
	Concrete	1.0×10^{-9}
	Aluminum oxide	1.0×10^{-13}
	Polystyrene	1.0×10^{-14}
	Polyethylene	$10^{-15} \sim 10^{-17}$

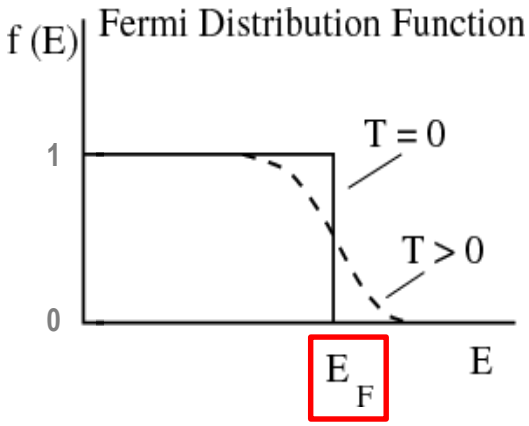
Unit: $[\Omega \cdot m]^{-1}$

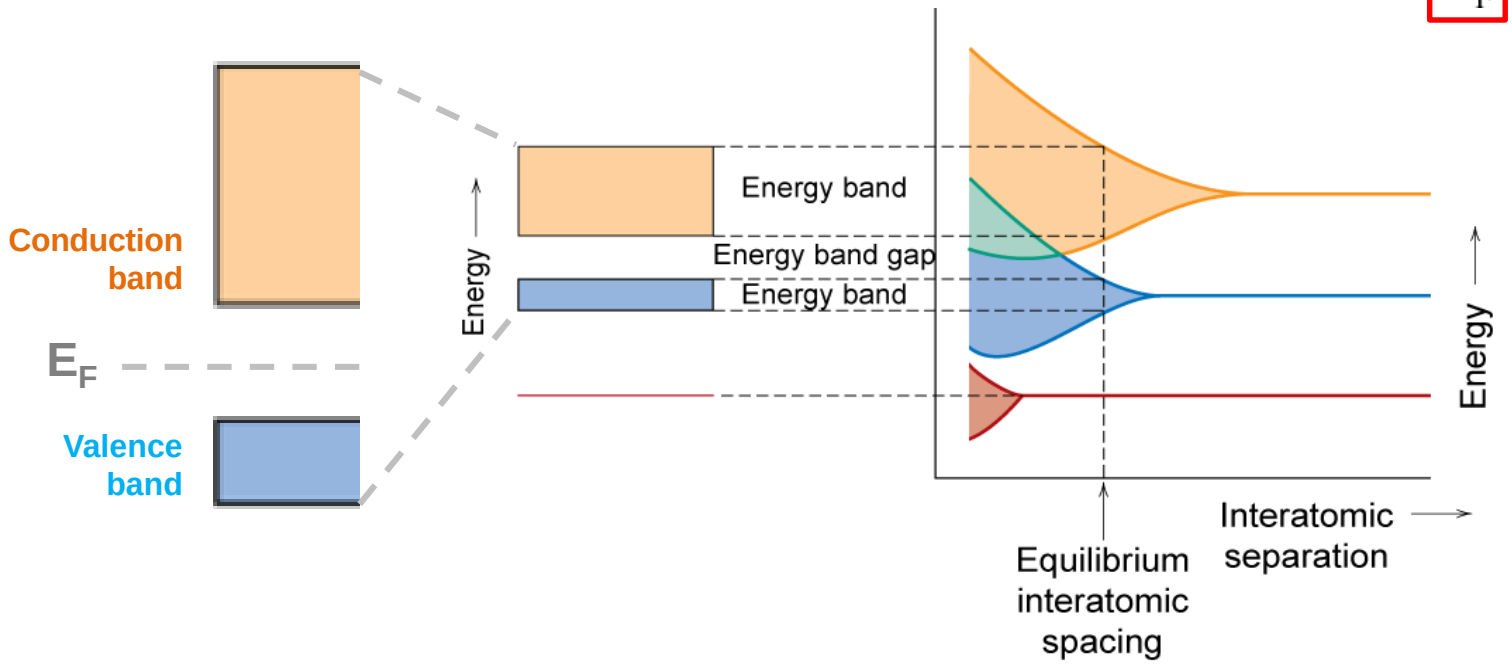
Energy Band structure



Energy Band structure

- **Conduction band**
  Electrons in valance band can jump up when excited
- **Valence band**
  The highest band where electrons occupy in ground state
- **Fermi Energy (E_f)**
  The highest energy level that an electron can occupy at 0K





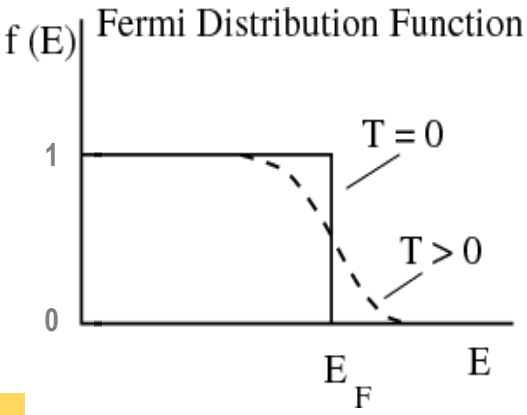
Adapted from Fig. 18.3, *Callister 7e*.

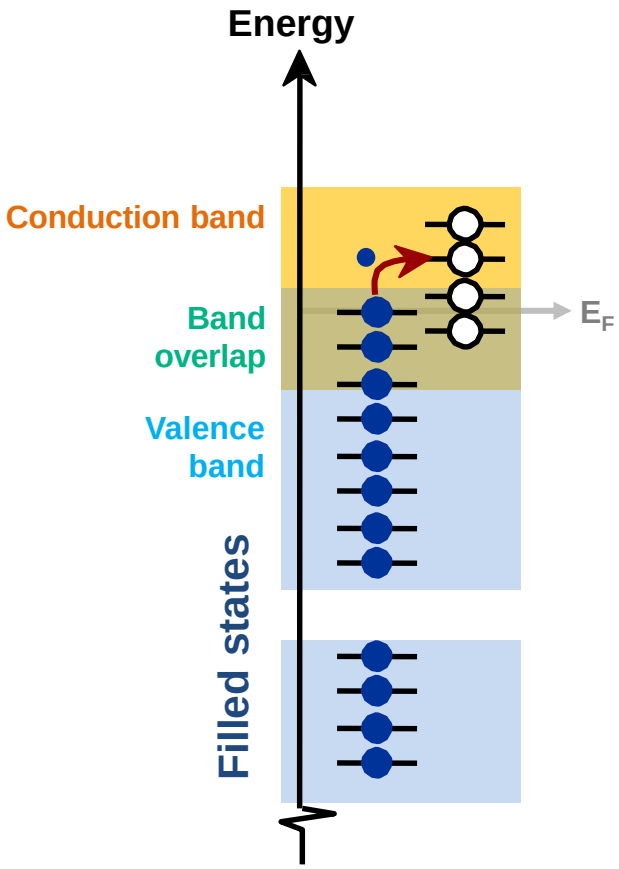
Energy Band structure

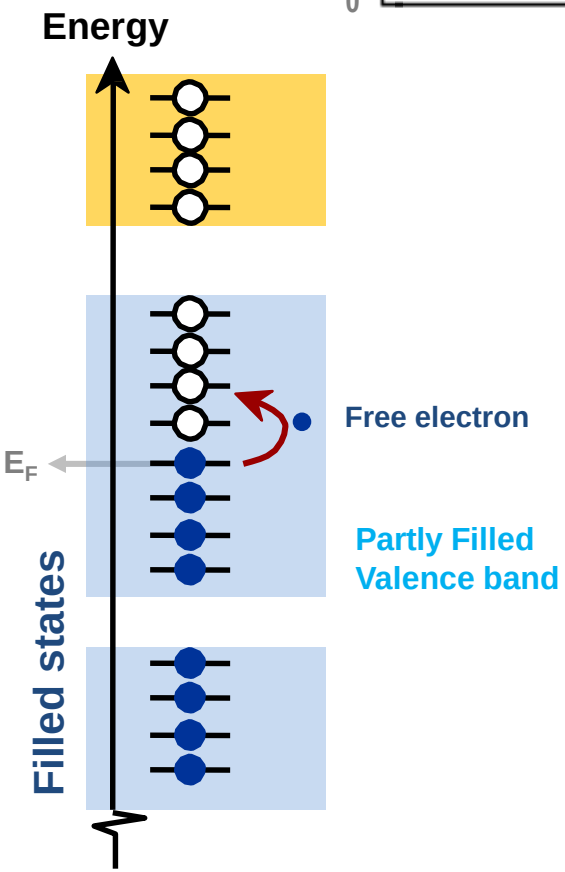
- **Conductors**

  Already have free electrons over 0K

  High conductivity







Energy Band structure

- **Semiconductors**

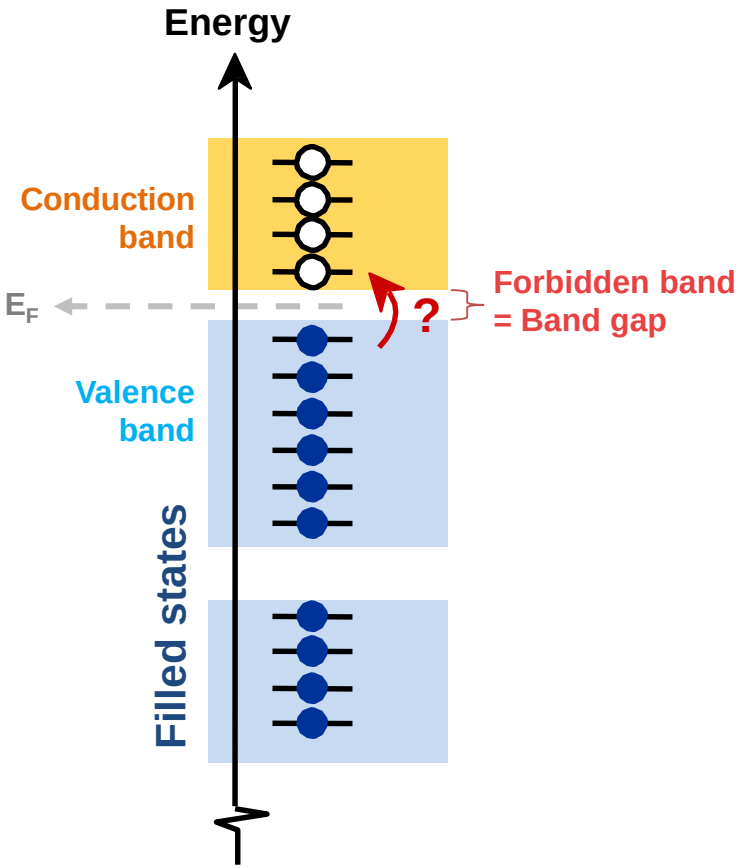
  Small band gap (<2 eV)

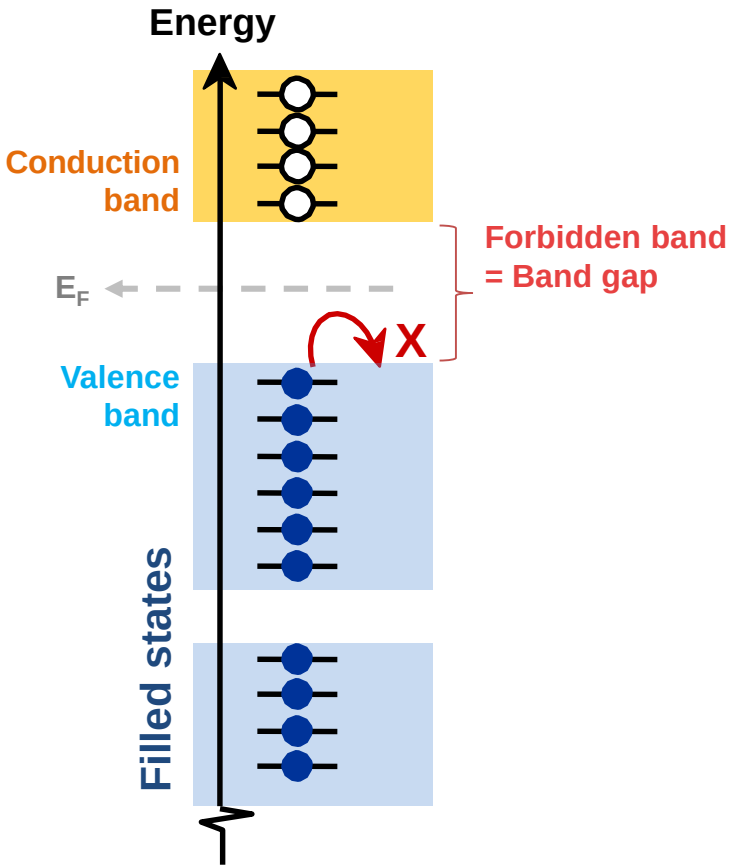
  고온 또는 광자 흡수 시 전도 가능

- **Insulators**

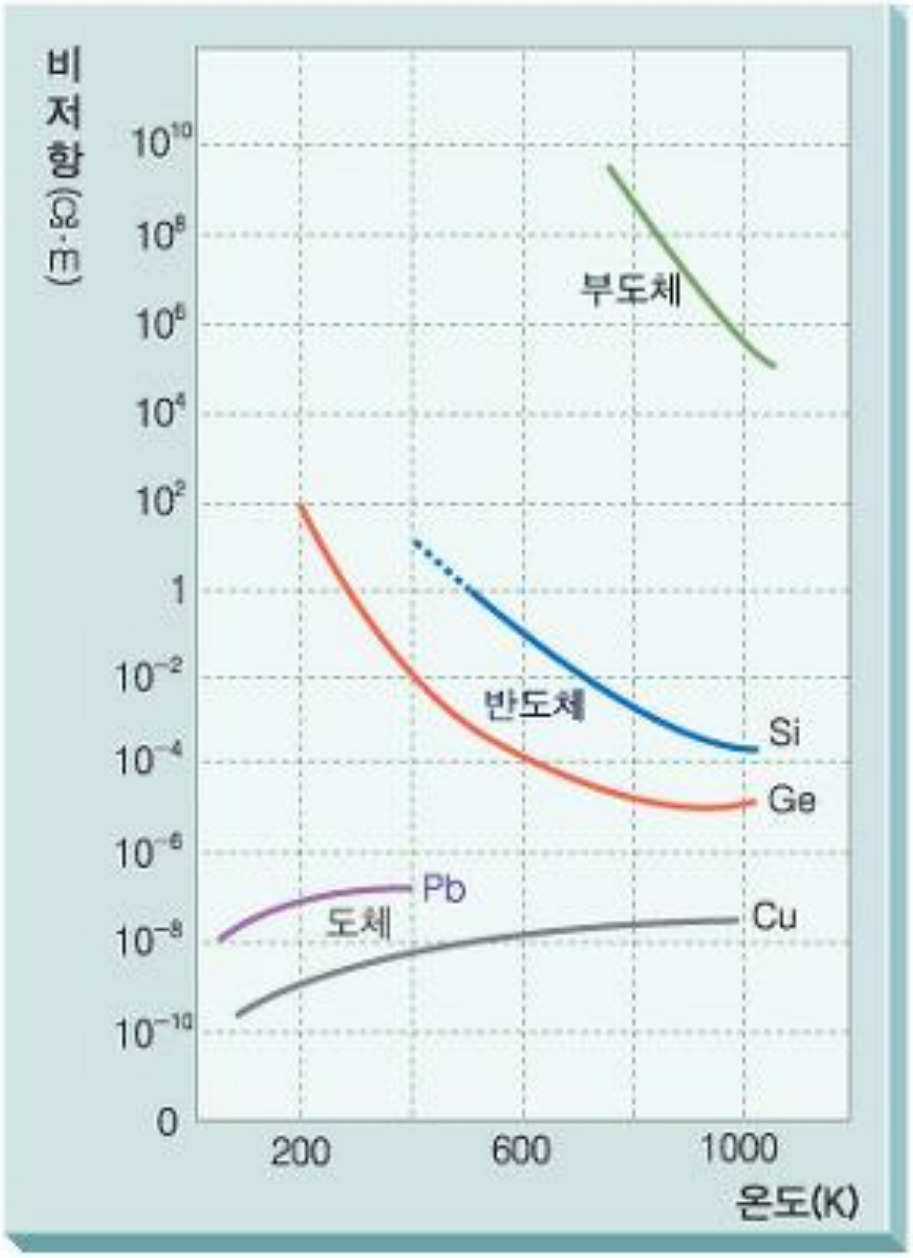
  Large band gap (>2 eV)

  전도 불가능, Very high resistivity





Resistance-Temperature Relation



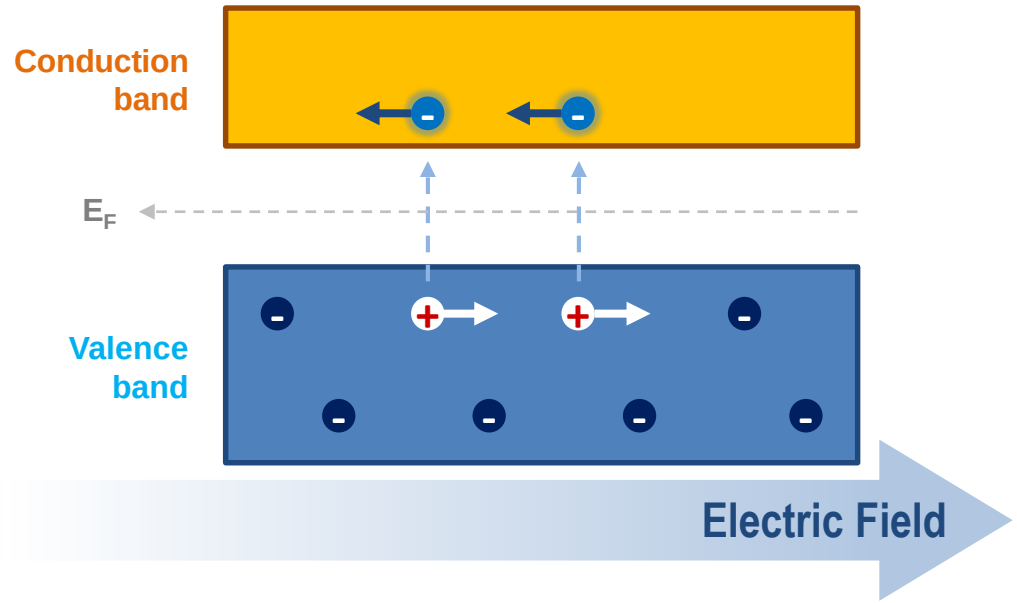
- **Resistance-Temperature Relation**

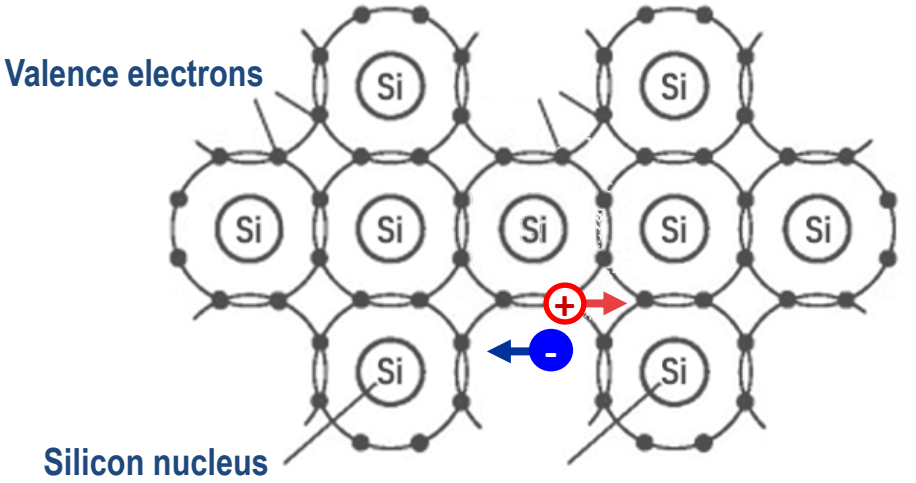
① $R_{insulator}$ & $R_{semiconductor} \propto T^{-1}$
∵ carrier concentration ↑

② $R_{conductor} \propto T$
∵ thermally vibrating lattice atoms

Charge Carriers

Conductivity of Semiconductors





- **Electron**

  (-) Charge Carrier

- **Hole**

  (+) Chage Carrier

- **Conductivity**

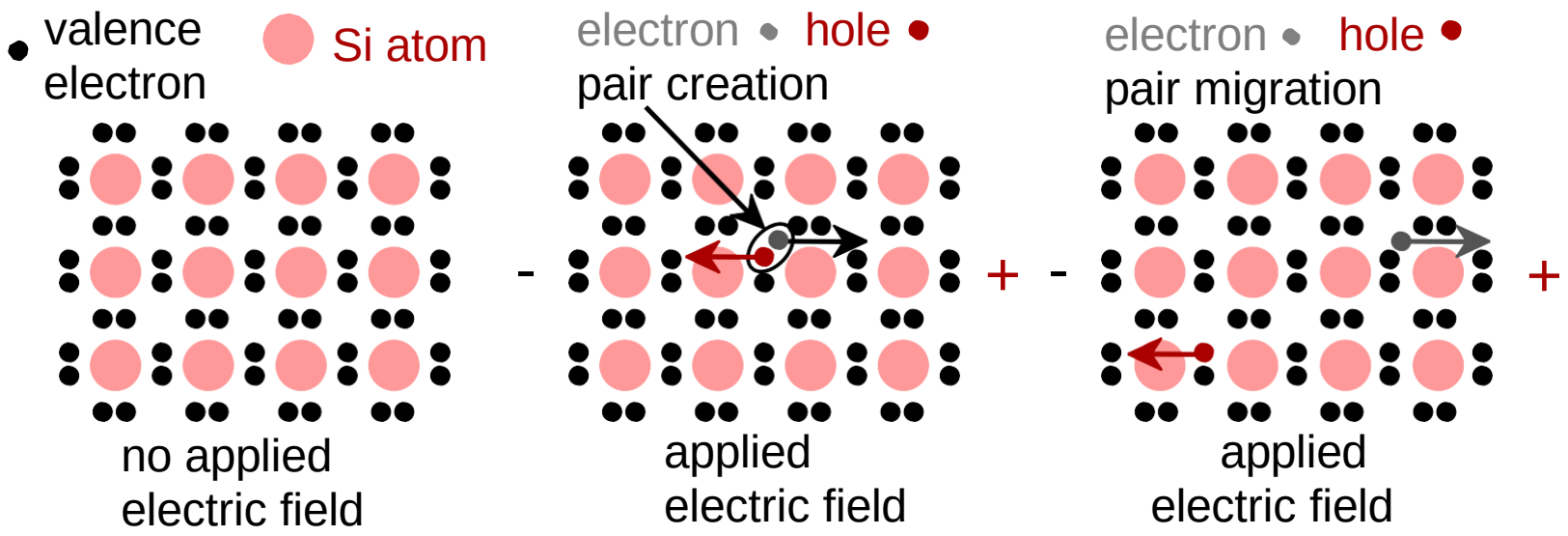
  $\sigma = ne\mu_e$

- **Mobility**

  $v_d = \mu_e E$

Adapted from Fig. 18.6 (b), *Callister 7e*.

Charge Carriers



Adapted from Fig. 18.11, *Callister 7e*.

- **Conductivity of semiconductor**

$$\sigma = ne\mu_e + pe\mu_h$$

hole mobility

electron mobility

Intrinsic & Extrinsic semiconductor

- **Intrinsic Semiconductor:**

  순수한 재료의 전자 구조에 의해 반도체 특성을 가지는 경우

  전자의 수 = 정공의 수 ($n=p$)

  예) Si, Ge, GaAs 등

- **Extrinsic Semiconductor:**

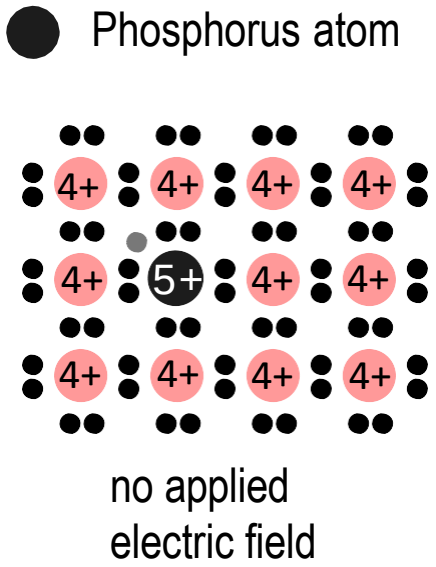
  도핑하여 extra 캐리어 (전자 또는 정공)를 부여

  N-type: n >> p

  P-type: p >> n

Intrinsic & Extrinsic semiconductor

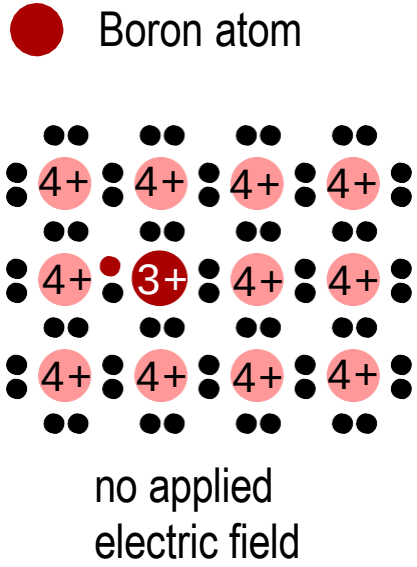
- ***n*-type (*n* >> *p*)**



no applied electric field

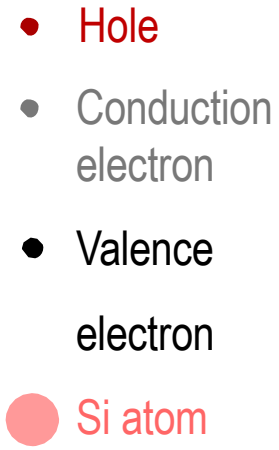
$$\sigma \approx ne\mu_e$$

- ***p*-type (*p* >> *n*)**



no applied electric field

$$\sigma \approx pe\mu_h$$

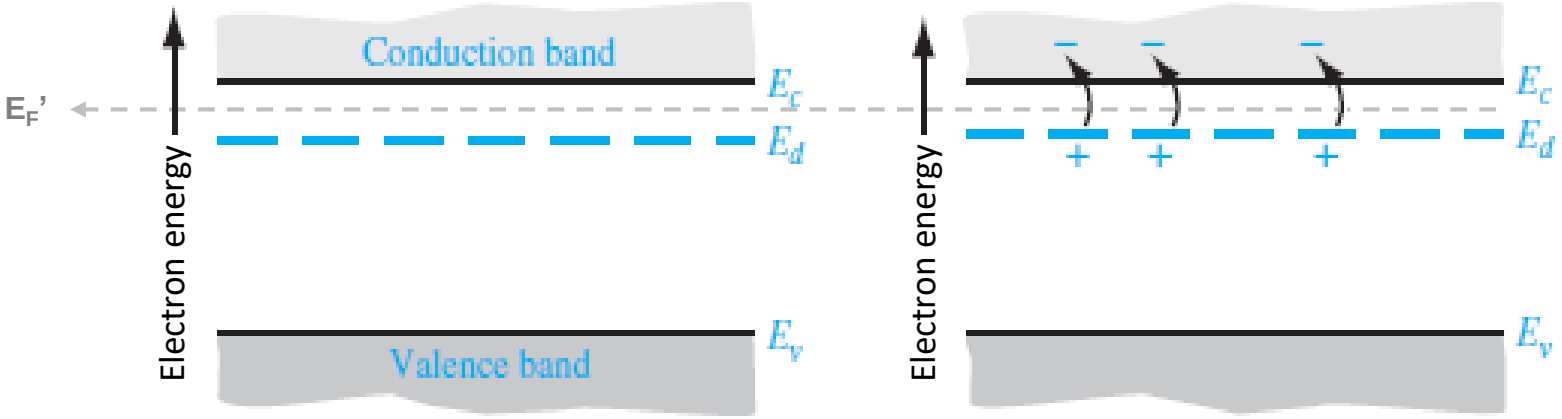


Adapted from Figs. 18.12(a) & 18.14(a), *Callister 7e*.

Intrinsic & Extrinsic semiconductor

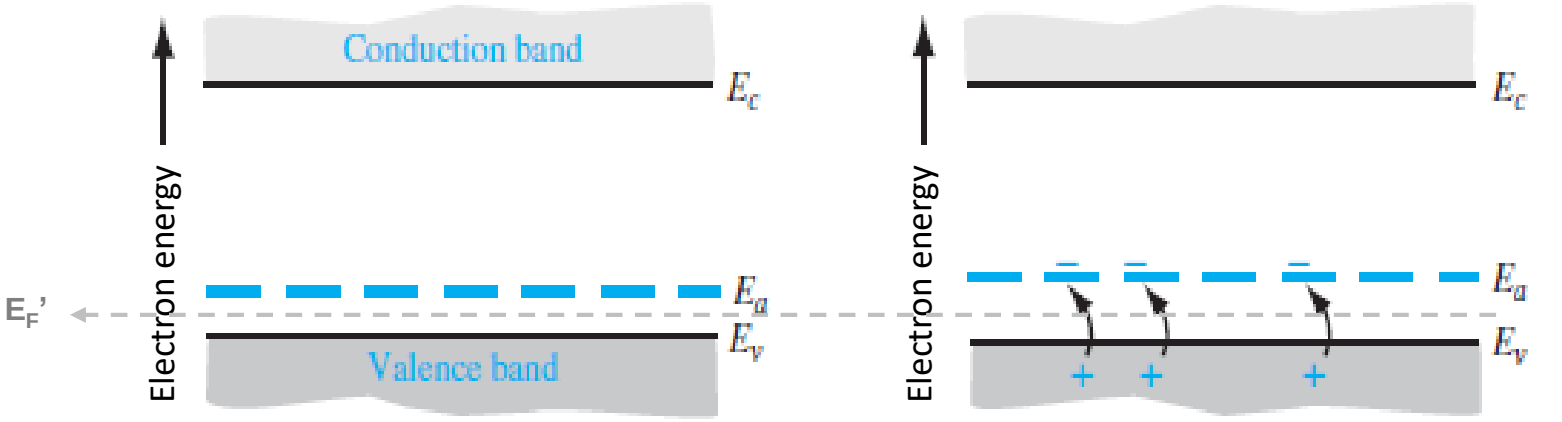
- ***n*-type**

Donor State → Conduction Band



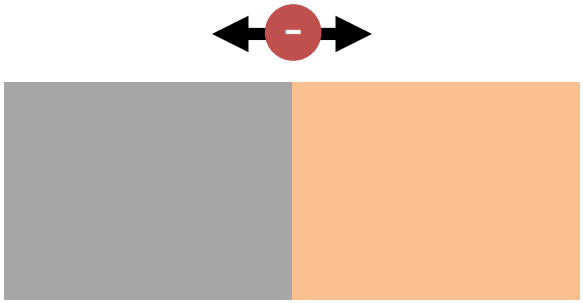
- ***p*-type**

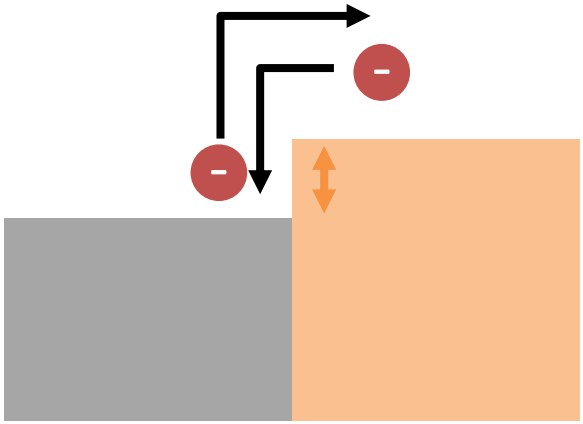
Valence Band → Acceptor State

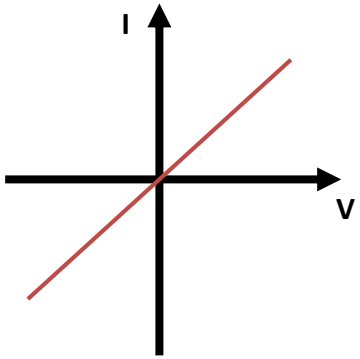


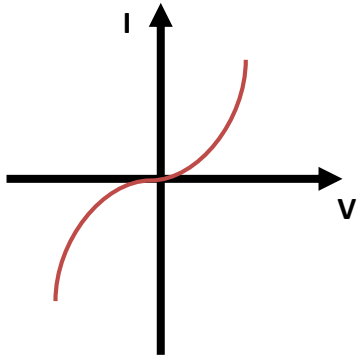
Ohmic Contact

- Ohmic Contact







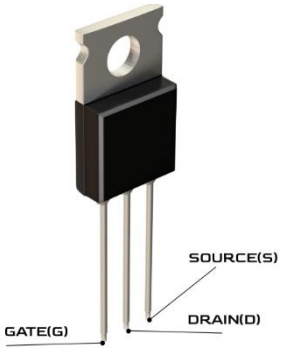


Ohmic Contact

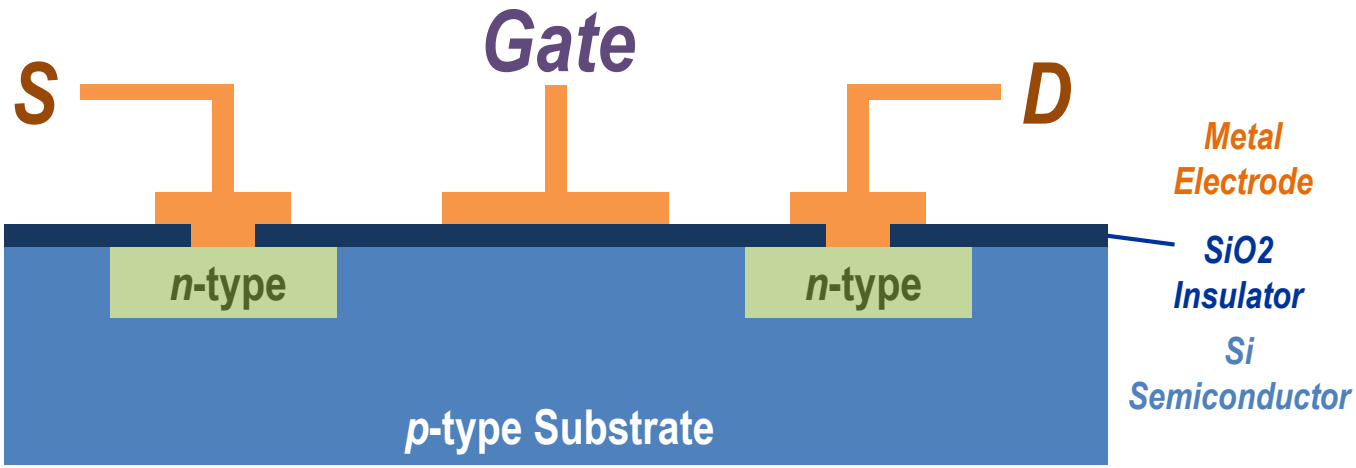
Non-Ohmic contact

MOSFET

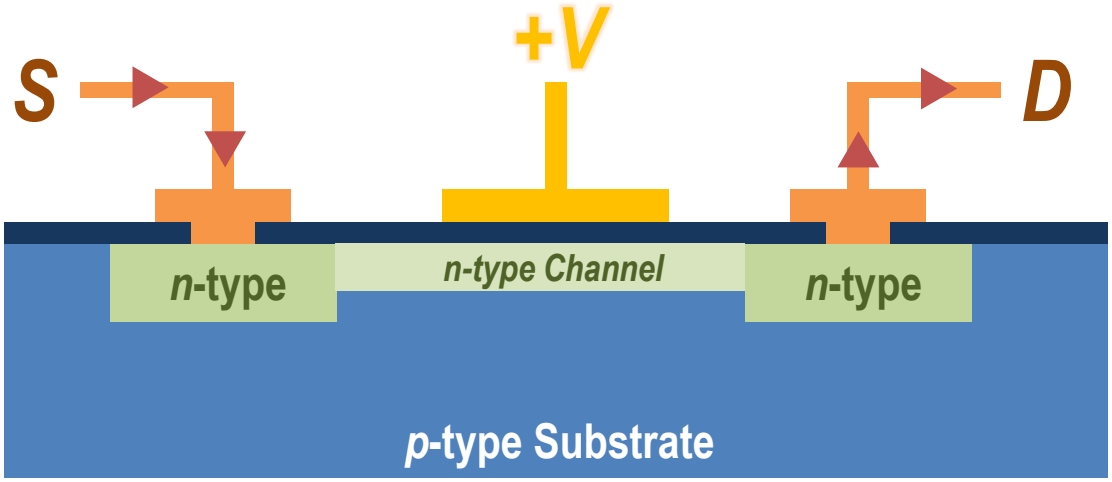
Metal Oxide Semiconductor Field Effect Transistor



V_{Gate}=0
OFF state



V_{gate}>0
ON state



Experiment

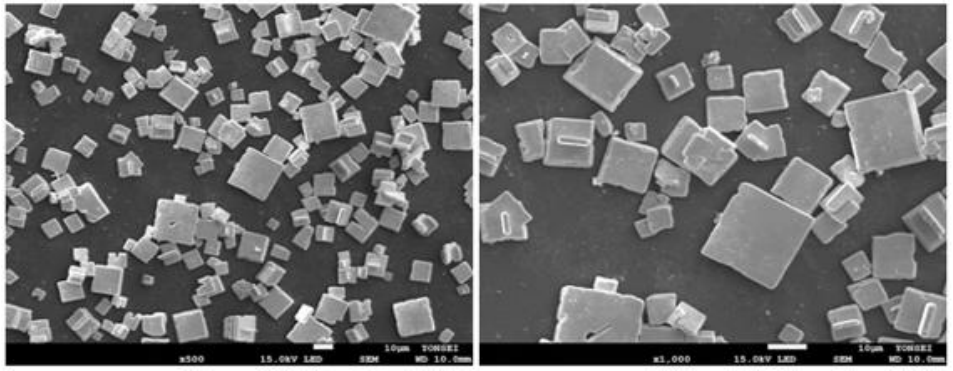
어떻게 저런 구조로 만들 수 있었을까?

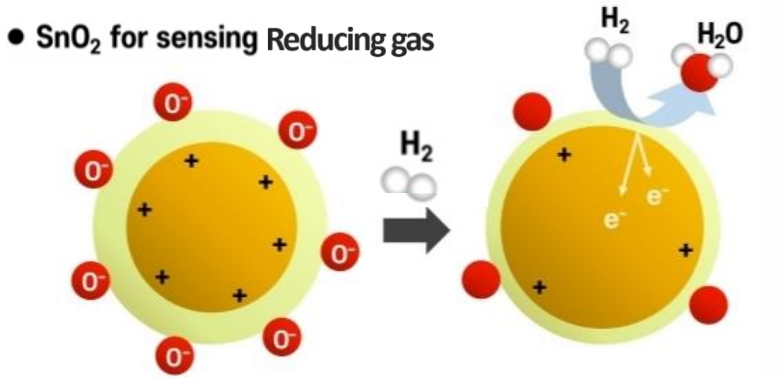
https://www.youtube.com/watch?v=AcDn4bvW5IU

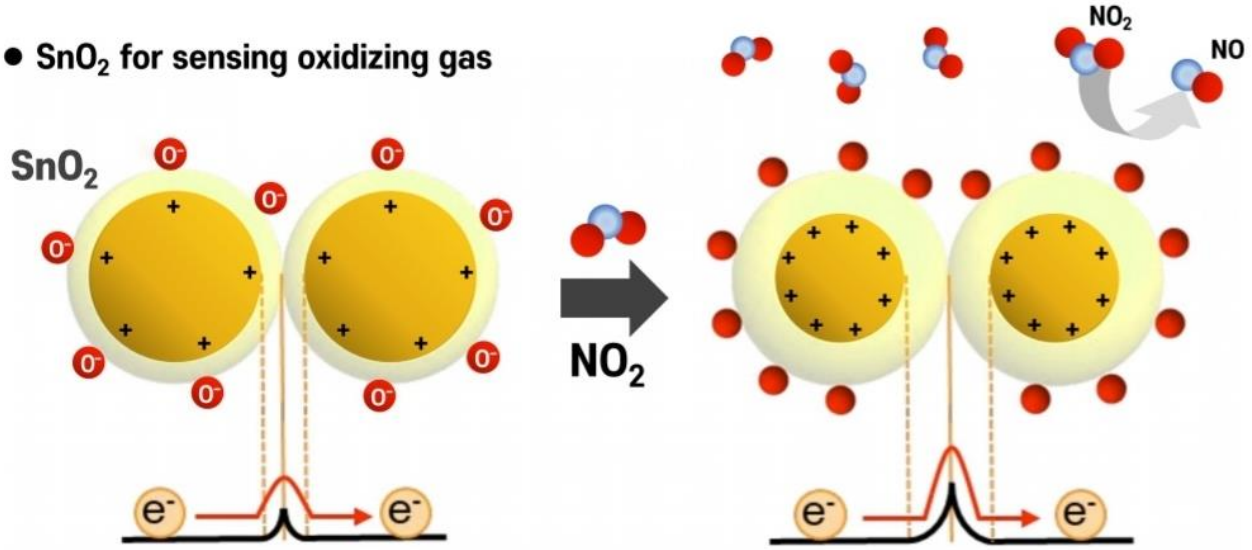
출처 : SK하이닉스 SK hynix

Experiment

Oxide Semiconductor Gas Sensor Mechanism





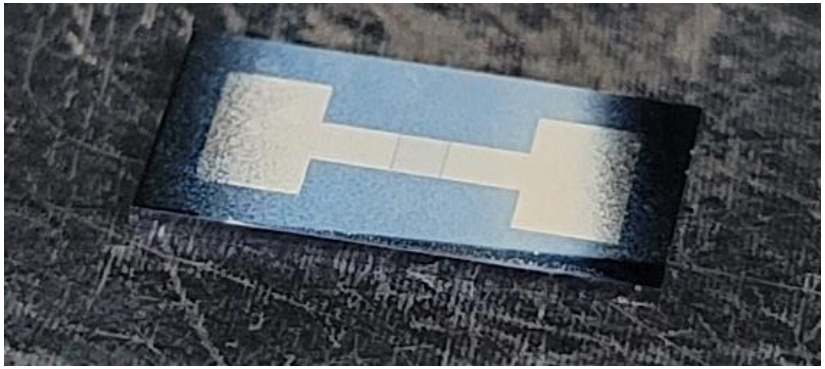


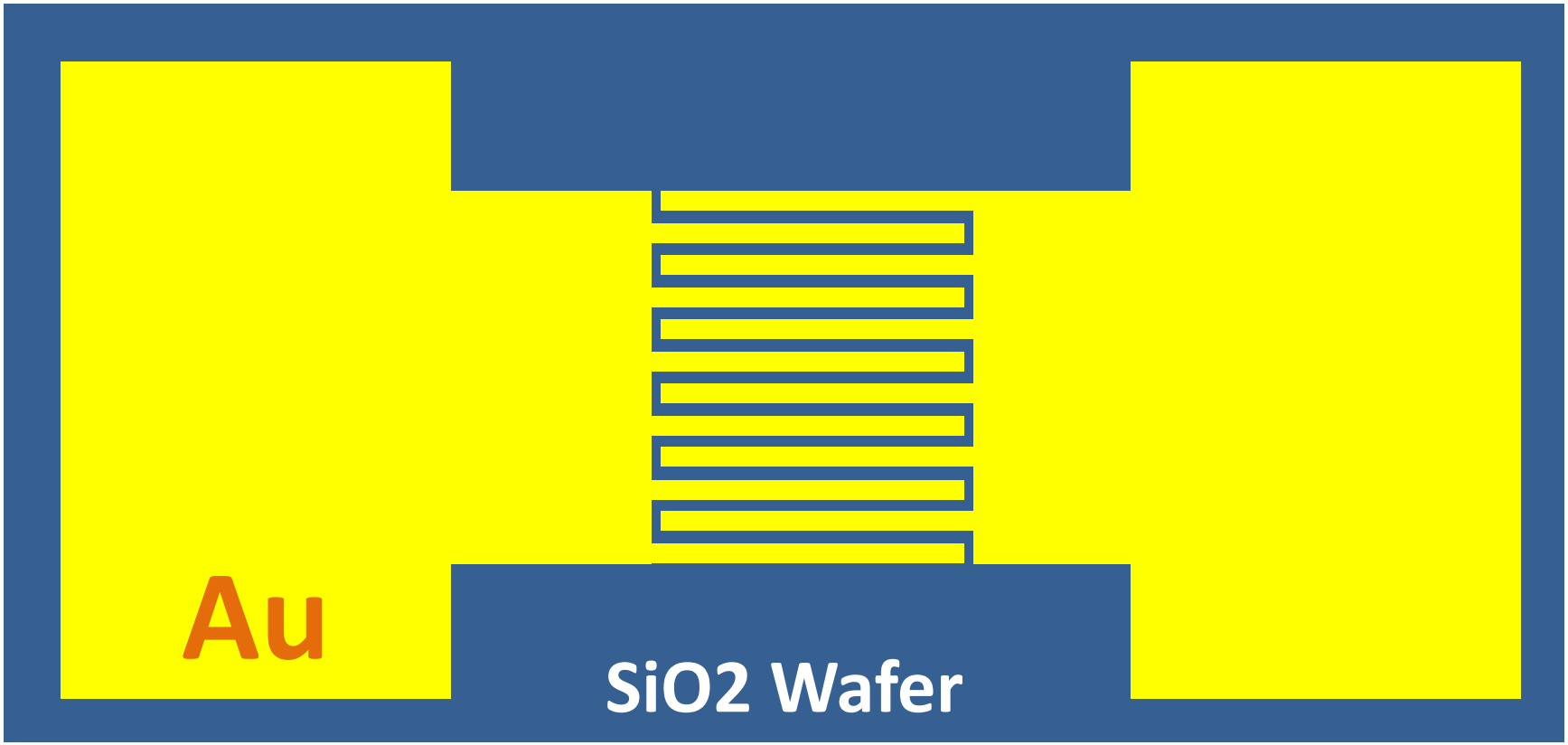
NO_2 exposure → Space charge layer expands → Resistance increases

Experiment

- IDE (Interdigitated electrode)

Fabricated by Sputter & Photolithography

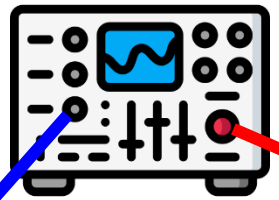


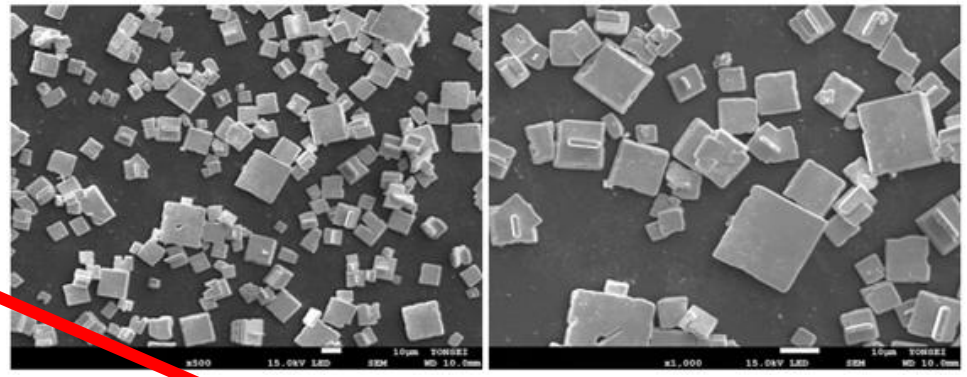


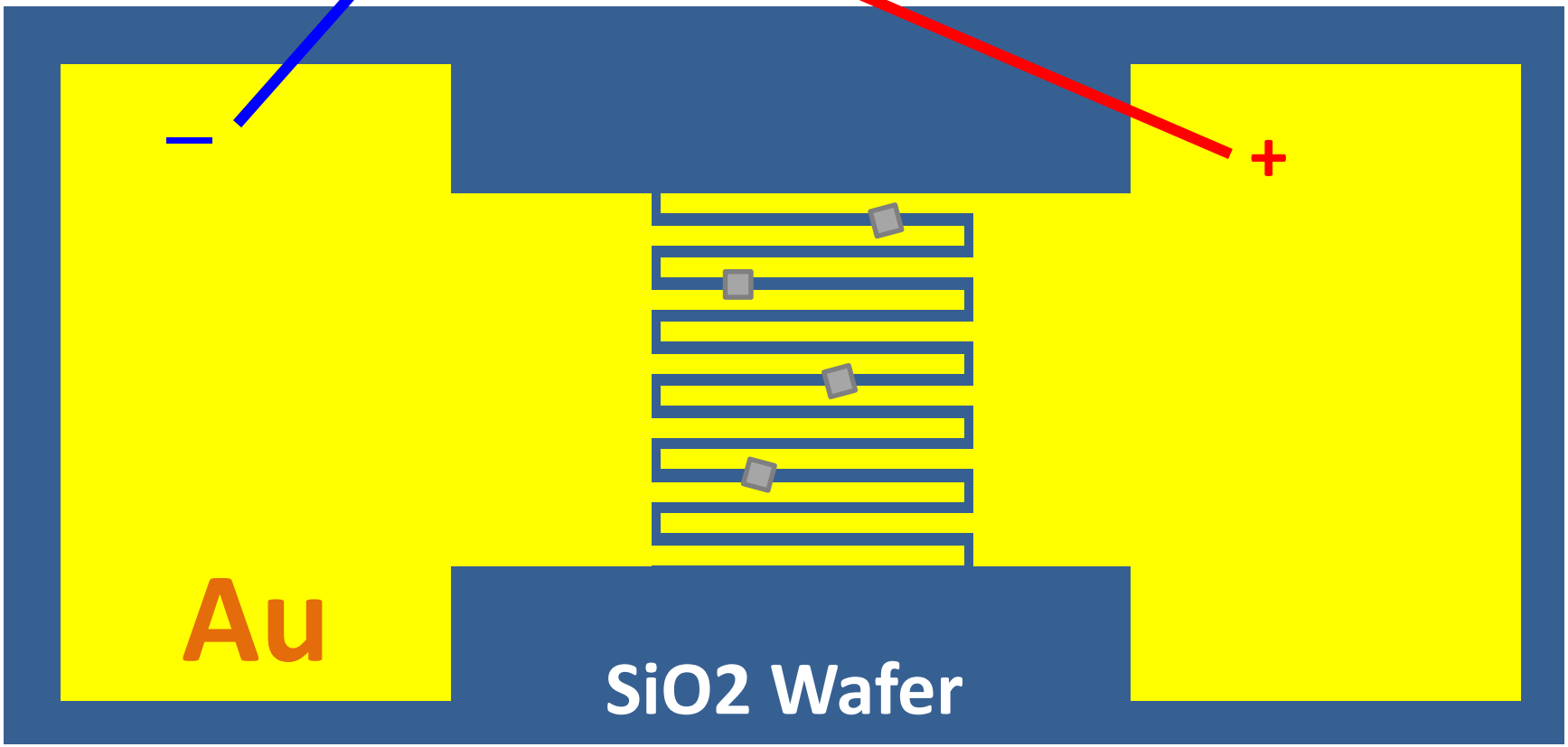
Experiment

IDE (Interdigitated electrode)

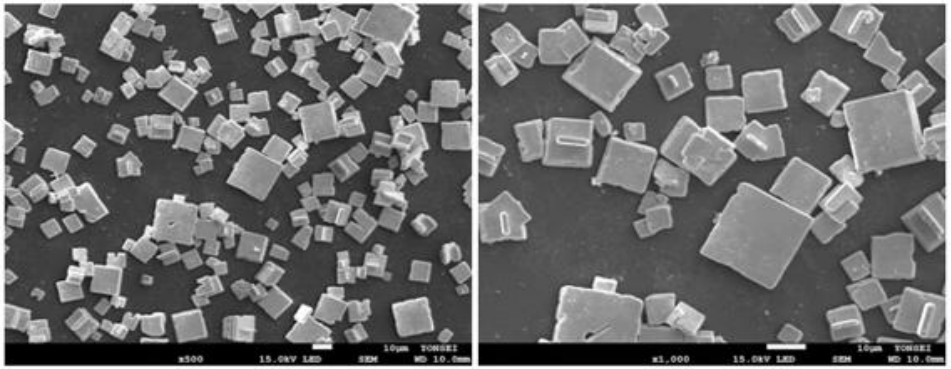
$$V = IR$$

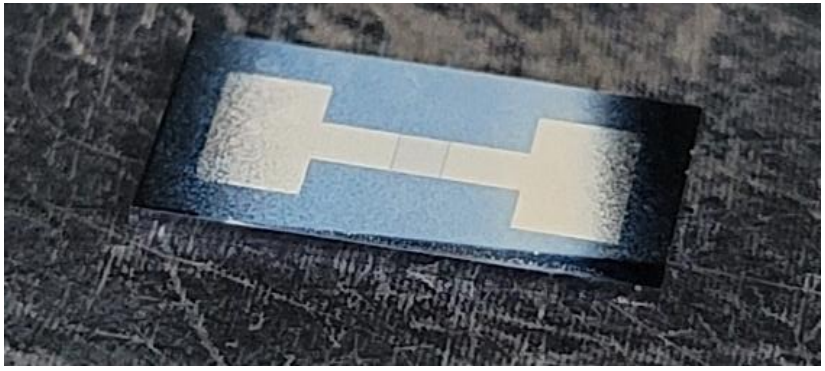


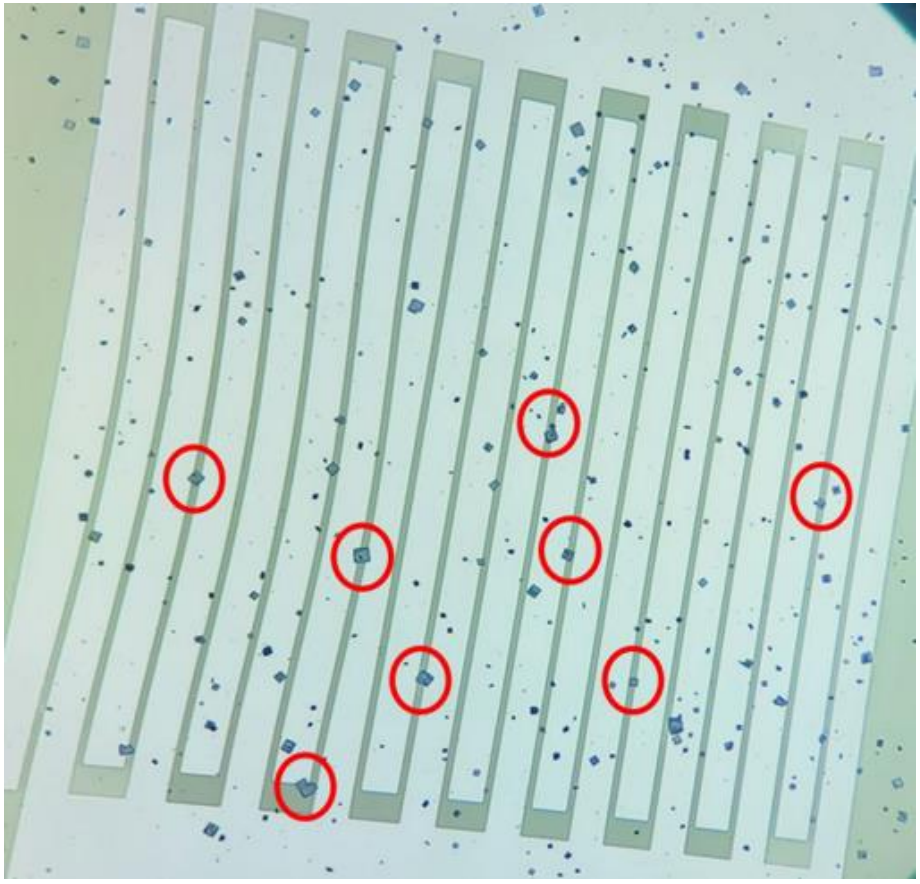


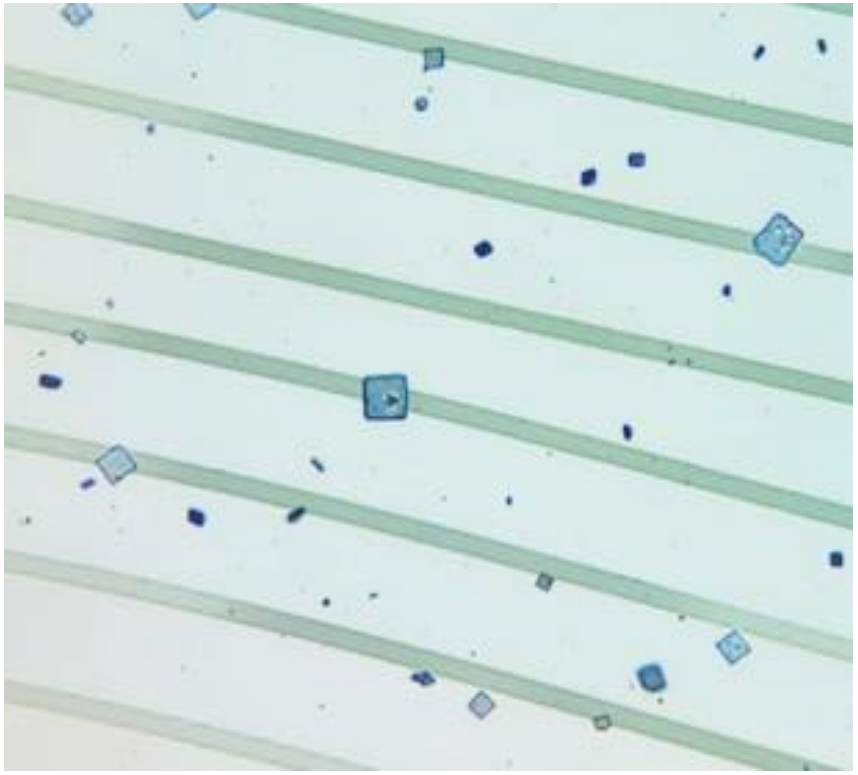


Experiment



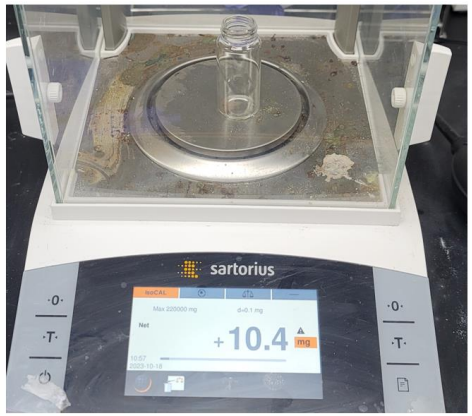


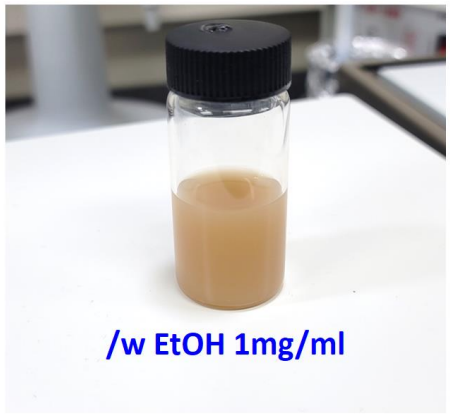


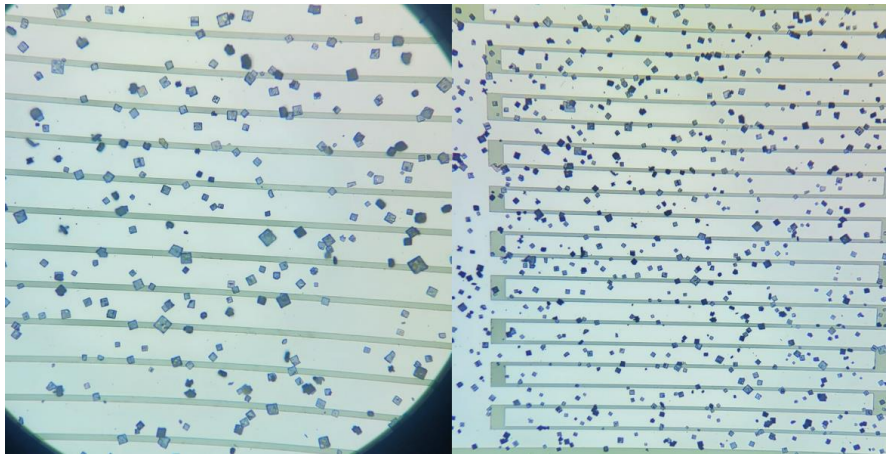


Experiment

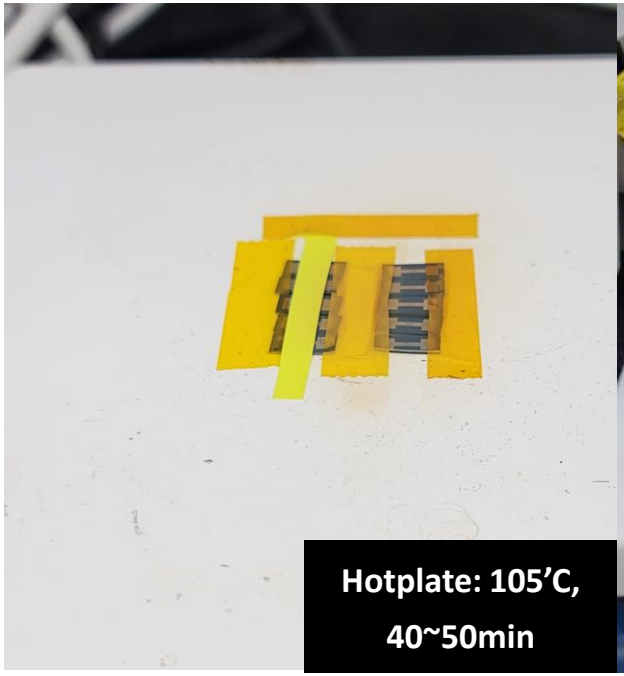
- Dispersion 용액 제작

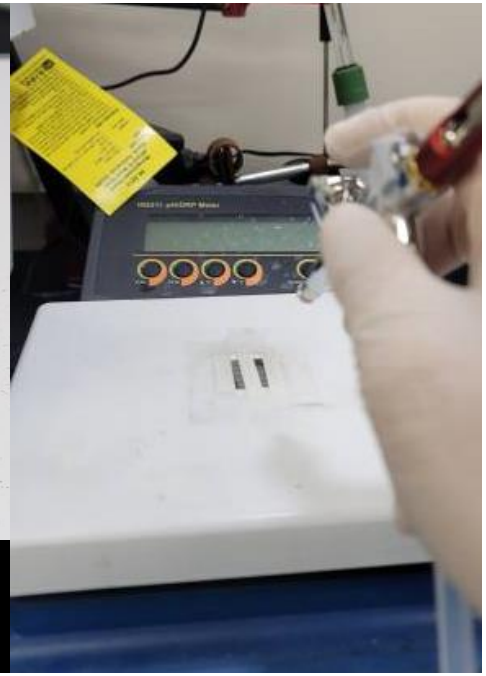


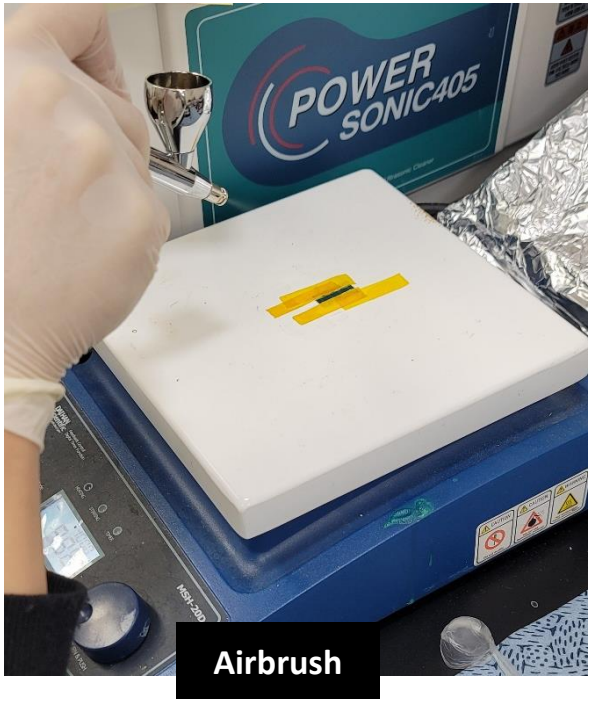




- Airbrush 진행

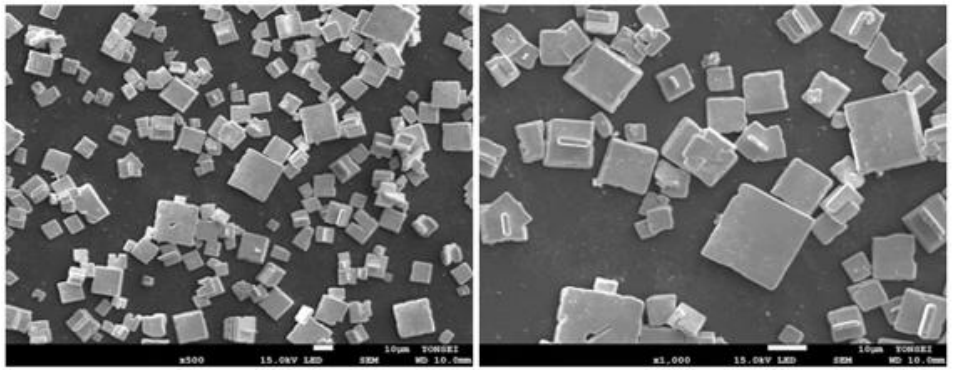


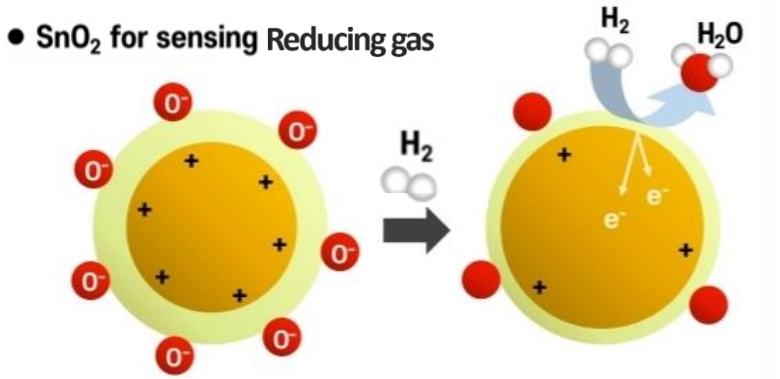


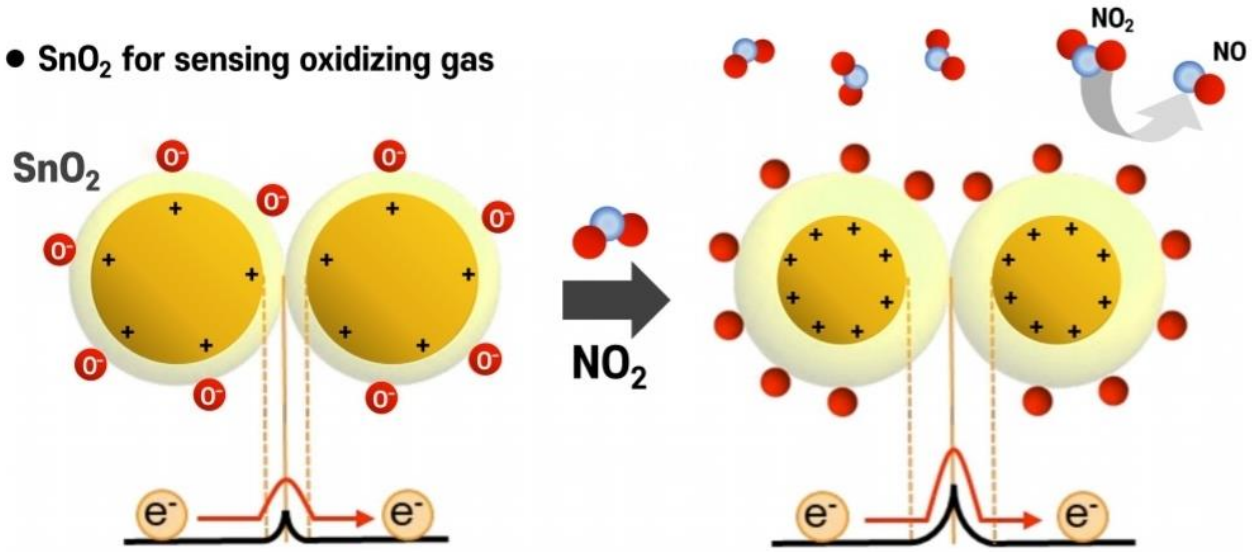


Experiment

Metal Oxide Semiconductor Gas Sensor Mechanism





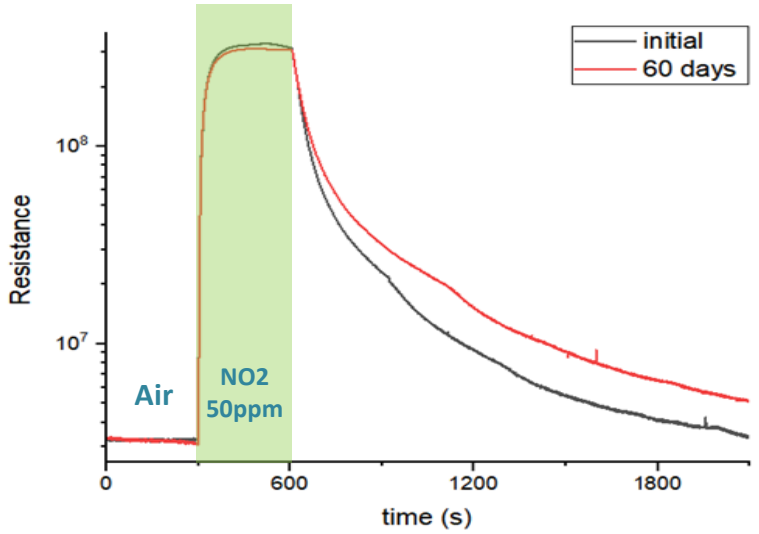


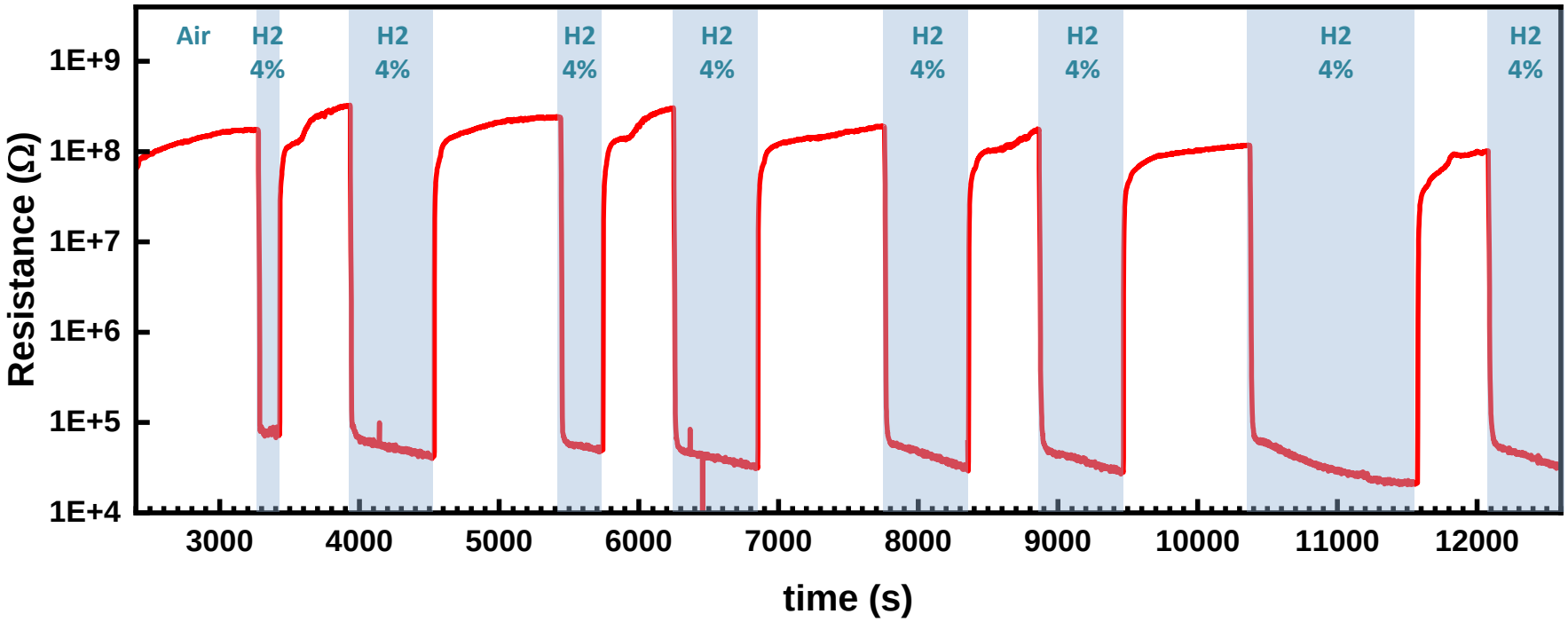
NO_2 exposure → Space charge layer expands → Resistance increases

Experiment

SnO-based gas sensor

Results (4% H2, 50ppm NO2)

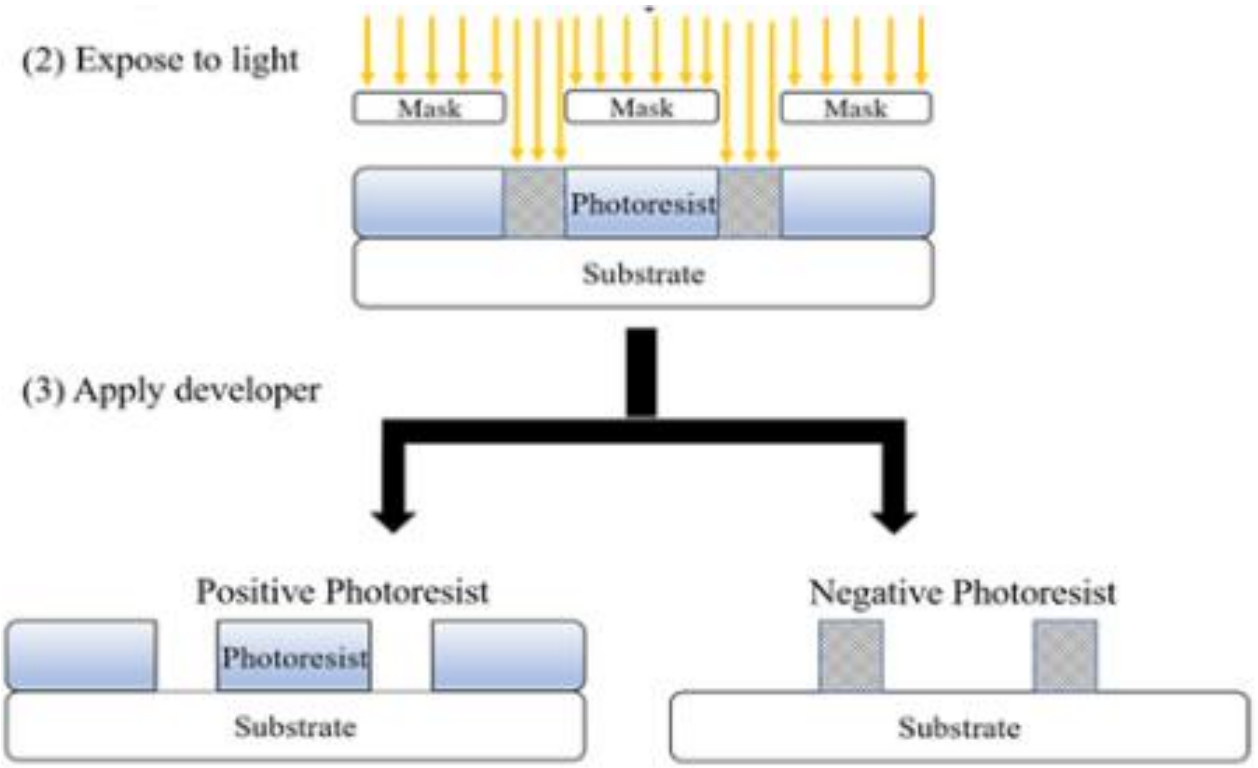




Experiment

- **Photoresist (PR)**

  특정 파장의 빛에 의해
  성질이 변하는 물질



- Positive PR

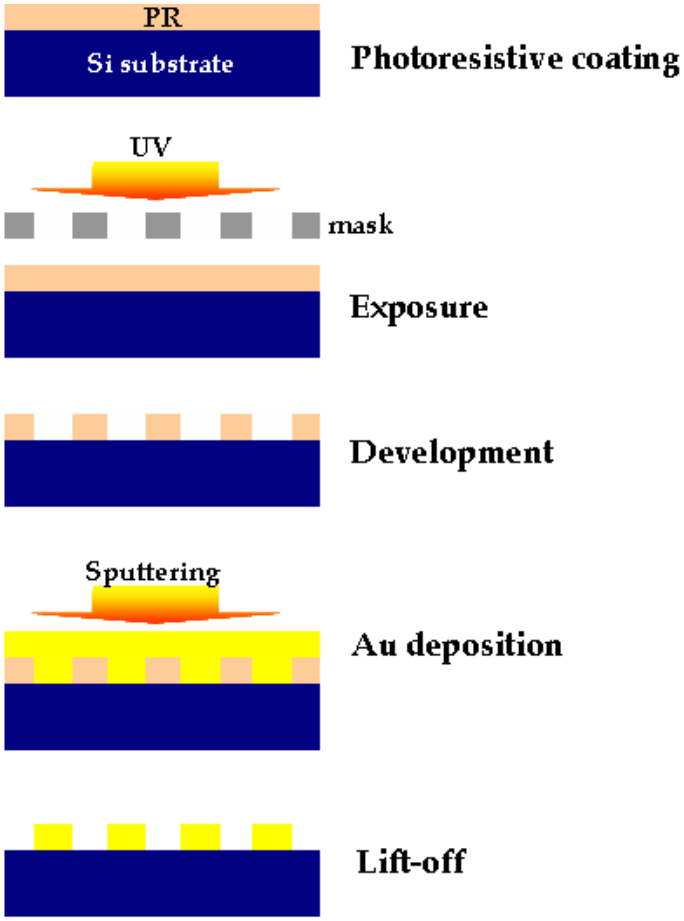
빛에 노출된 부분이 화학적인 분해로 인해 **Developer**에 씻겨 나감.
즉, Mask로 덮여 빛이 닿지 않은 부분이 남는다.

- Negative PR

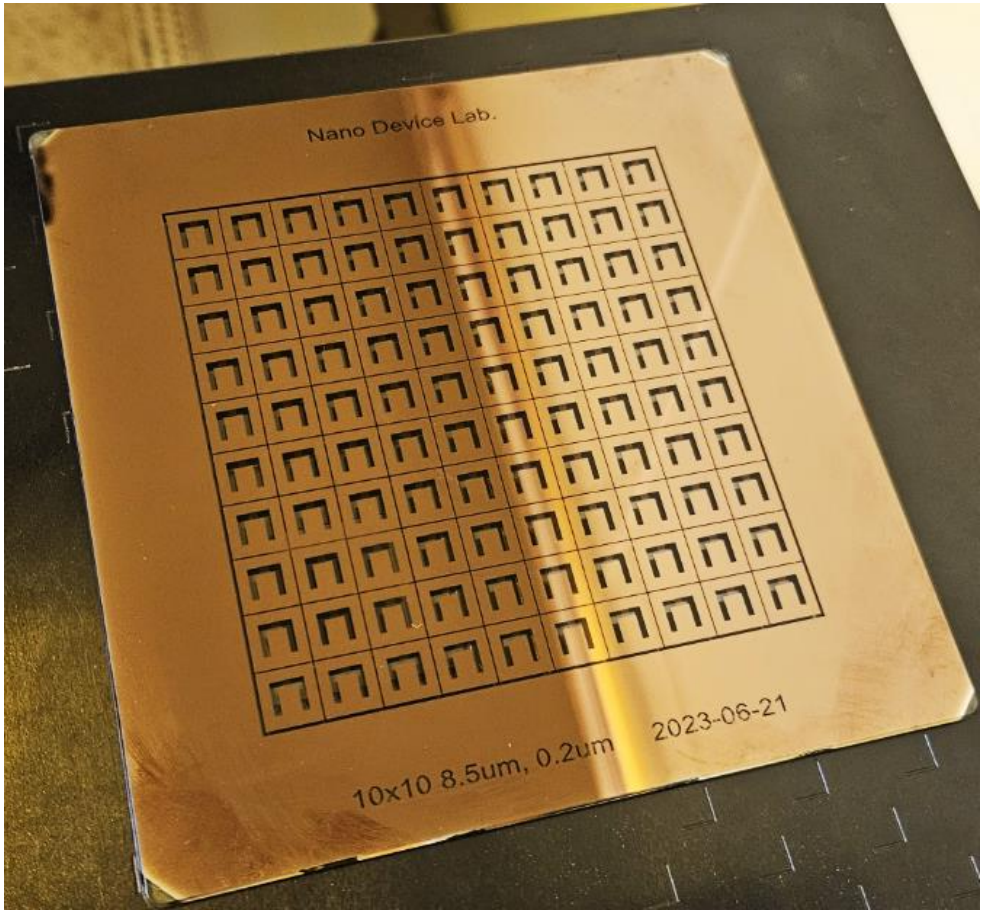
빛에 노출된 부분이 화학적인 결합으로 인해 **Developer**에 씻겨 나가지 않음.
즉, Mask로 덮어 빛이 닿지 않은 부분이 용해된다.

Experiment

- **Photolithography**
  (Lift-off Process)

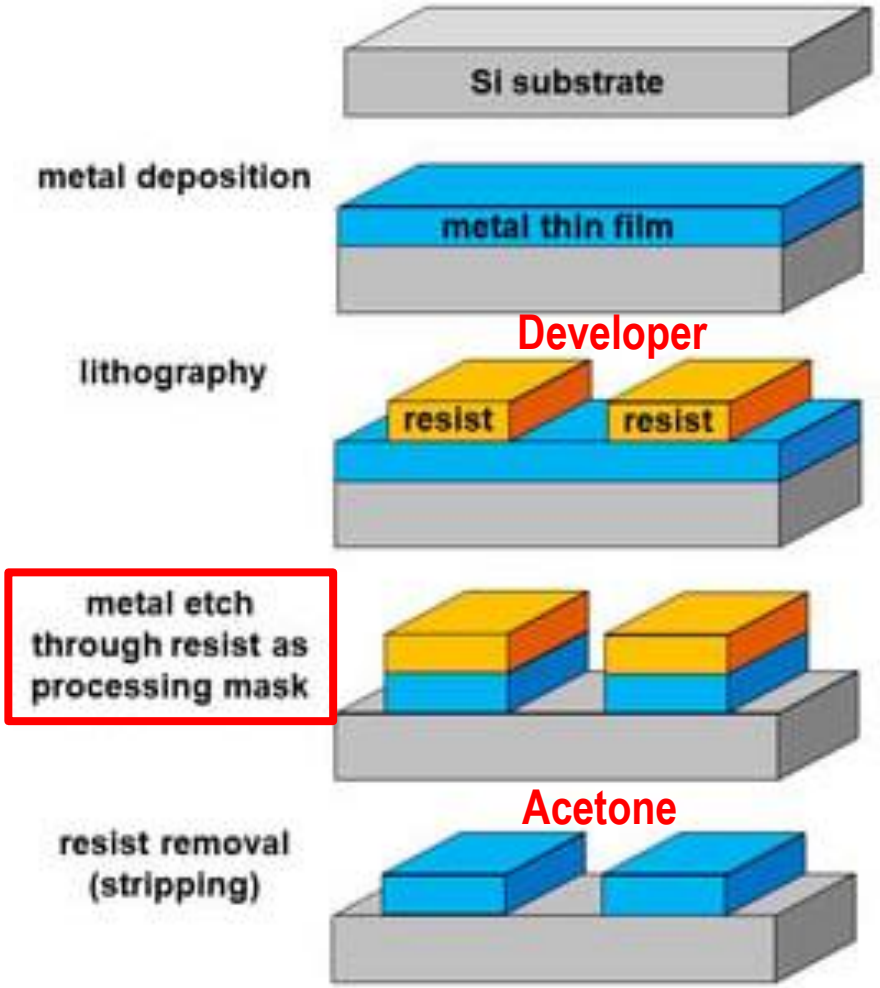


- **Photomask**

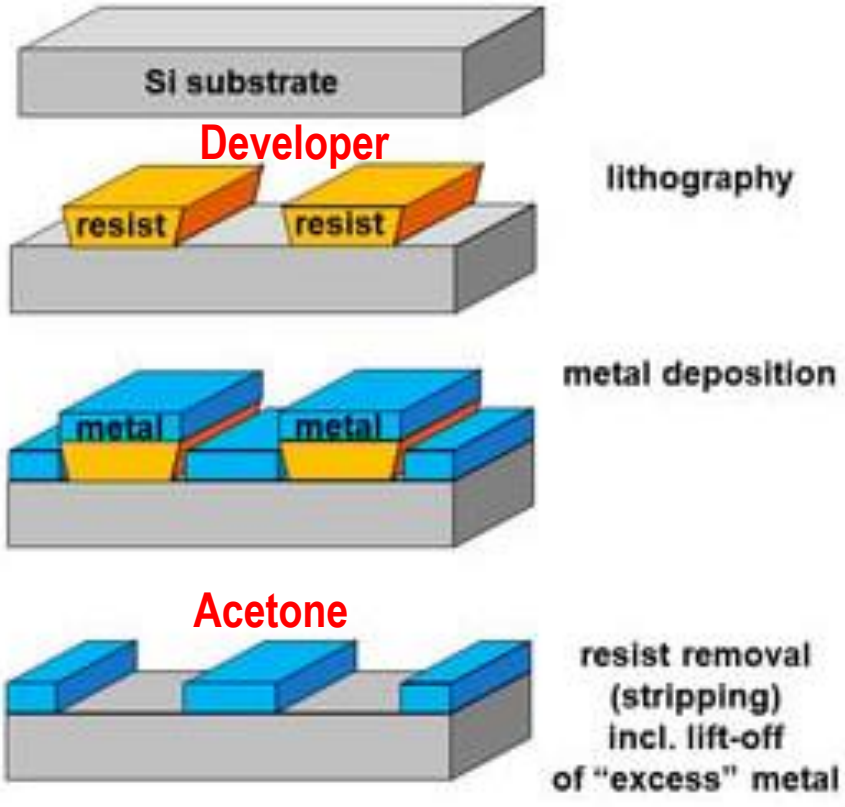


Experiment

Etch-back Process



Lift-off Process



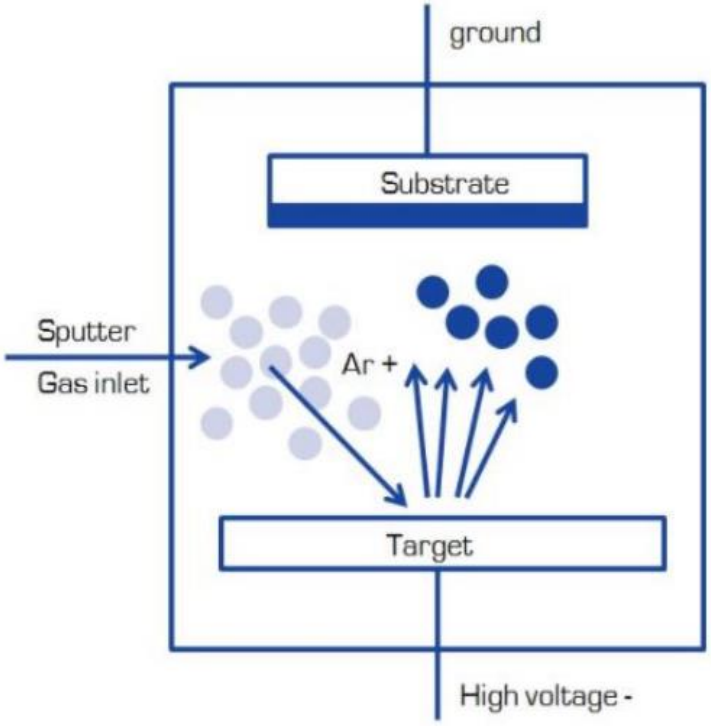
더 간단하지만
PR 두께가 두꺼워야 함

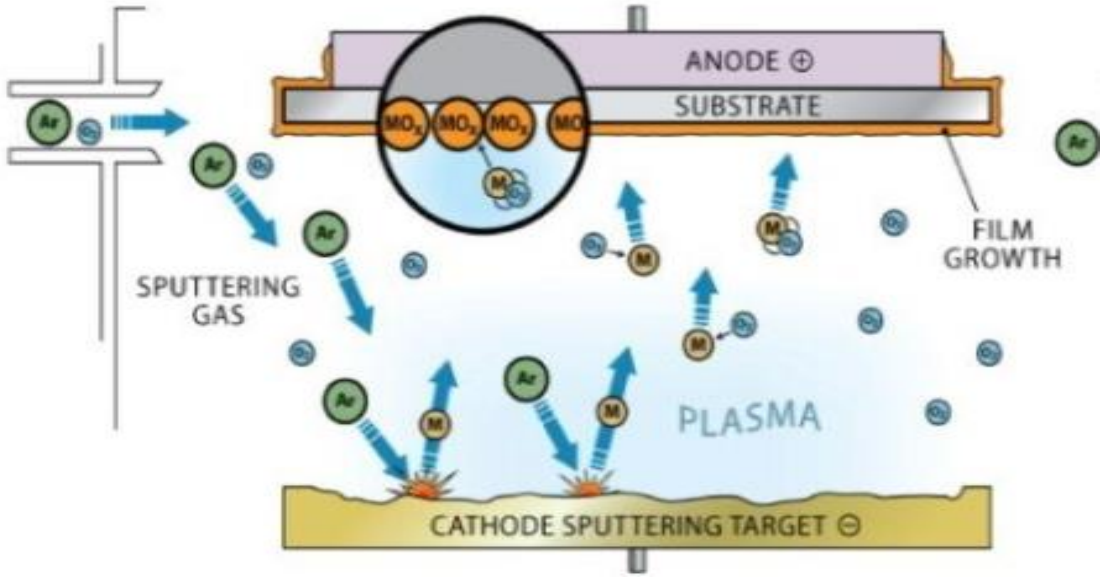
→ 미세패턴 형성 어려움

Experiment

- **Sputtering**

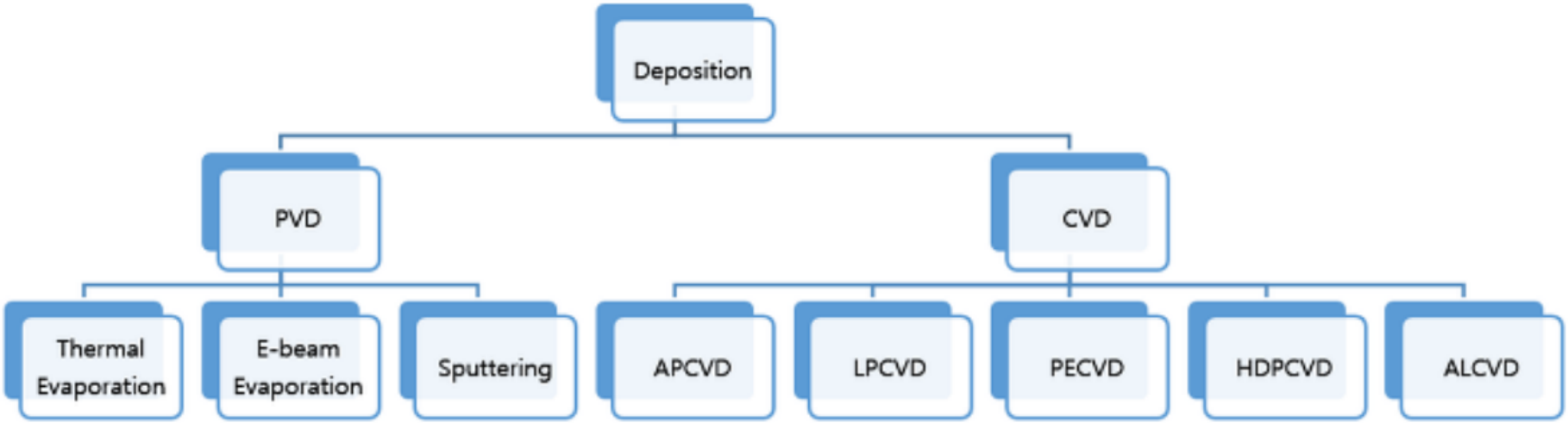
  이온화 된 가스 원자(Plasma)를 강한 전기장을 통해 타겟(Metal)에 충돌시켜 기판에 **금속 박막**을 형성하는 기술.





Target: Au, Ag, Pd, Pt, Cr…

Experiment



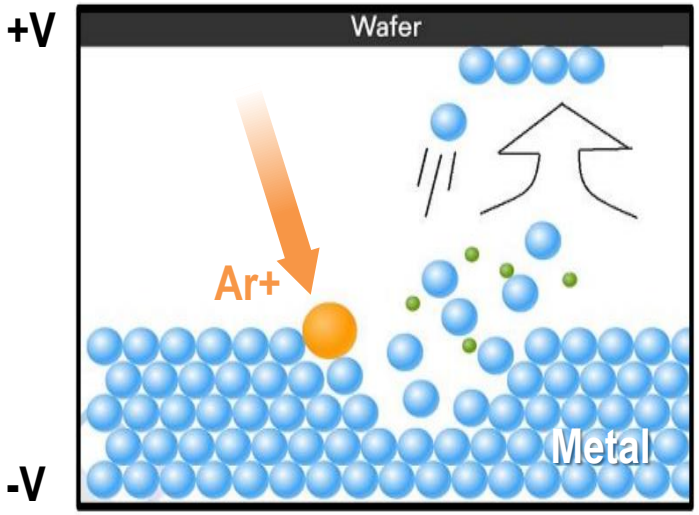
- **Sputter는 PVD (Physical Vapor Deposition)의 일종이다.**

① 챔버 내 Vacuum 조성

② 전자빔으로 Plasma 생성 (Ar+)

③ 고전압으로 Ar+ 가속 → 타겟(음극) 충돌

④ 튀어나온 타겟 Fragment가 기판에 증착



Experiment

실험 (이번주 목) - 센서 소자 구현을 위한 IDE 제작

1. Photolithography (공B331)

① Si 기판 위에 Photo Resist 물질을 도포한다

② IDE 포토마스크를 이용하여 UV exposure 진행

③ Developer를 통해 UV 노출된 PR 제거

④ OM으로 관찰

2. Sputter & PR Removal (첨단관 지하 2층 214)

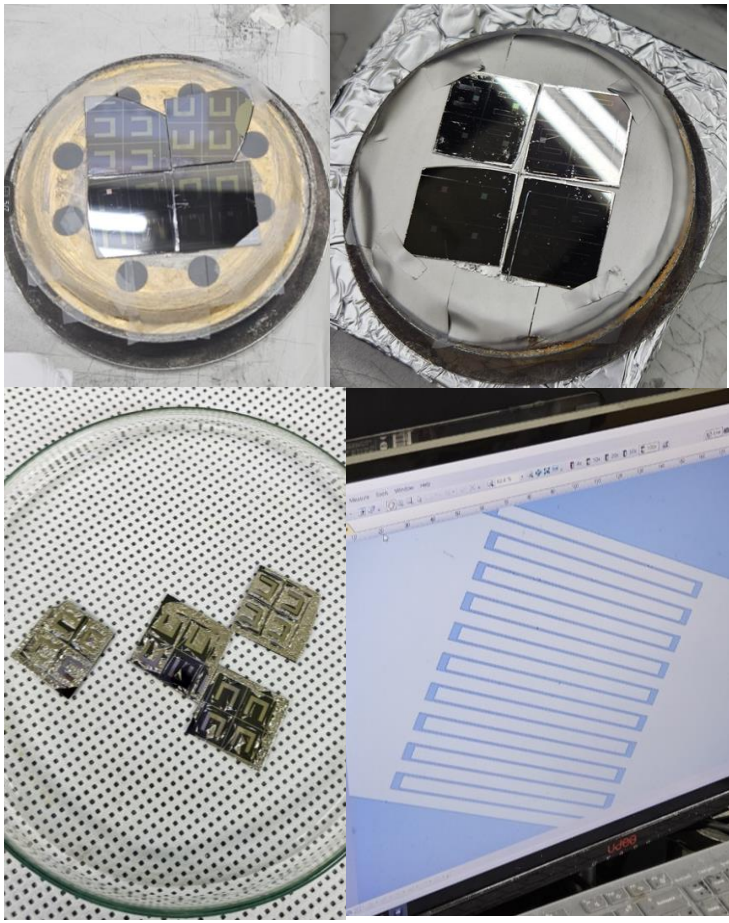
① PR 패터닝된 샘플을 스퍼터에 로딩

② 고진공을 잡는다

③ Ar 흘려주어 플라즈마 환경 조성 후 Au 박막 증착

④ 샘플 언로딩 후 Acetone에 담가 남은 PR을 제거한다.

④ OM으로 관찰



이론 및 실험 관련 퀴즈 (다음주 화)

재료의 전기적 성질

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